

Clari-D™

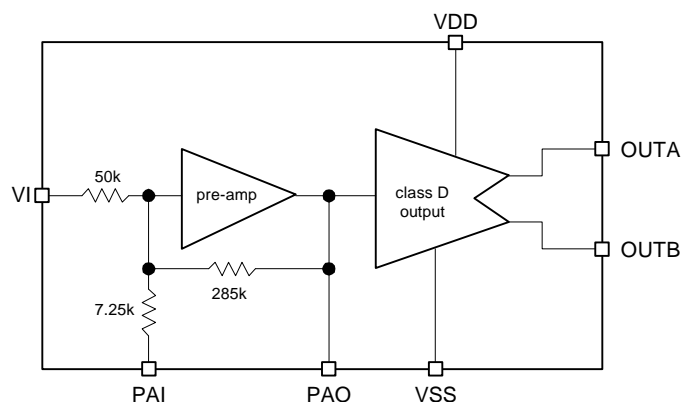
The Next Generation of Clear Sound Technology

Class D Output Amplifier - Model L272

Product Data Sheet

Features	Benefits
RTI's Unique, Patented Clari-D™ Class D Drive Technology	Clearer-sounding, efficient, low drain output amplifier for CIC to BTE applications
Adjustable gain with external resistor (32 dB range of adjustment)	Matches the gain of integrated receivers; improves application flexibility
Small size: 0.042 x 0.072" [1.07 x 1.83mm]	Integrate into favorite amplifier package without a significant space penalty
Available in Au-bump Chip or Hybrid with internal supply decoupling cap	Remove the class D driver from the receiver and save in repair costs
Break-before-Make Output Bridge	Less power supply ripple, reduced need for decoupling capacitance (approximately 10% of the capacitance compared to class D integrated receivers)
Low Output Noise (nominally 71uV rms total at maximum gain - 40uV rms when gain is reduced to minimum)	Quieter than integrated receivers - perfect for low-gain CIC applications

Block Diagram of L272 IC



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Absolute Maximum Ratings

Parameter	MIN.	MAX.	Units
Supply Voltage, Vcc		4	V dc
Operating Temperature	10	40	°C
Storage Temperature	-20	70	°C

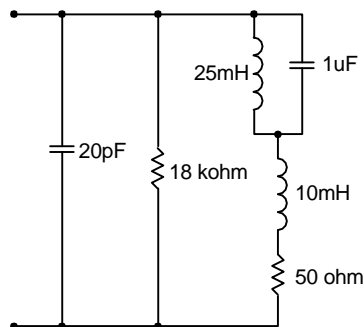
Electrical Characteristics

Conditions: T = 25°C, Vcc = 1.25V, f = 1kHz, except where noted

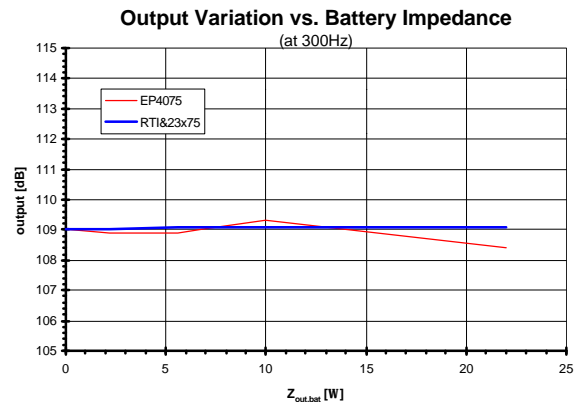
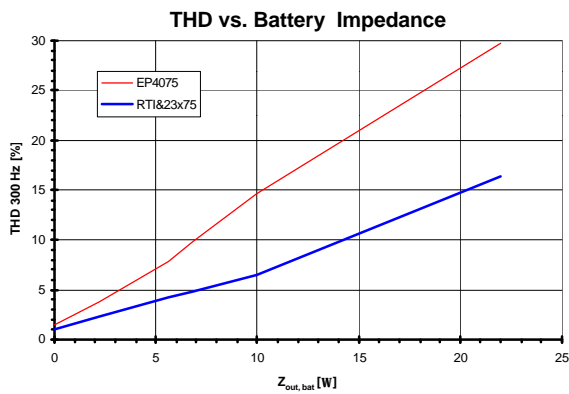
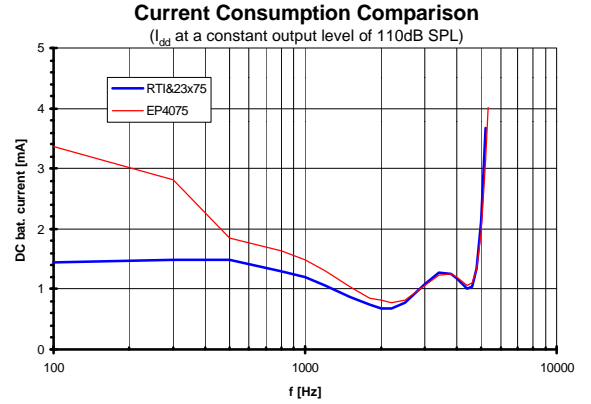
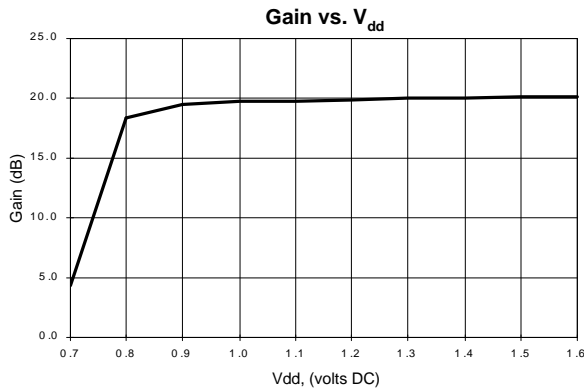
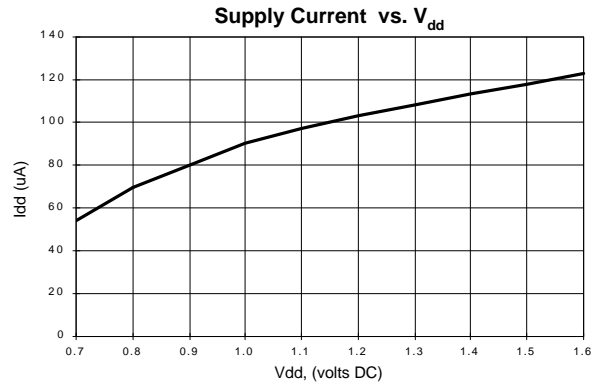
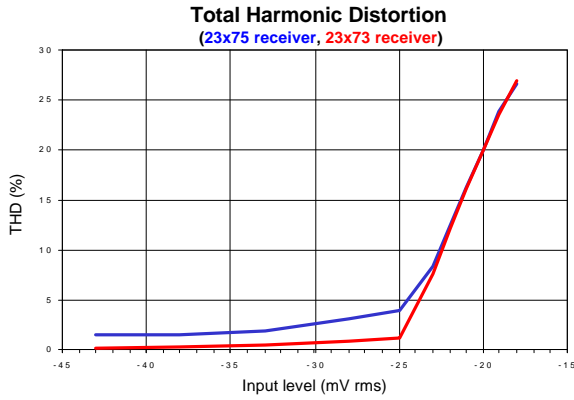
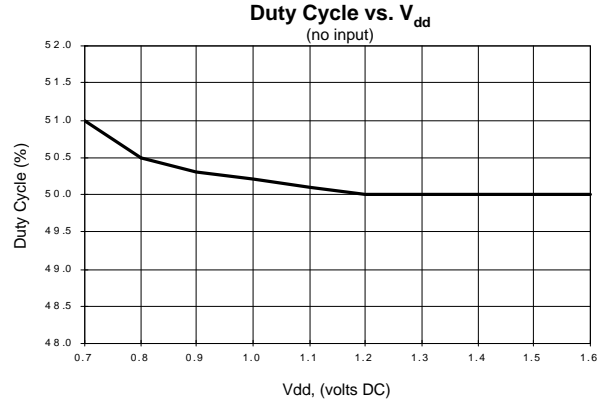
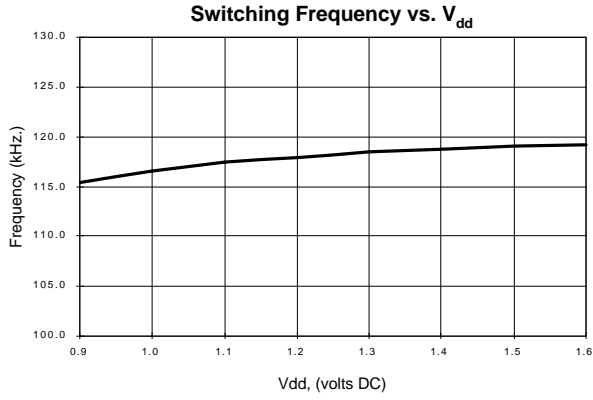
Parameter	Conditions	MIN.	TYP	MAX.	Units
Overall					
Supply Voltage, Vcc		1.05	1.2		V dc
Quiescent Current	no load, no input		110	TBD	μA
Icc under load	Inductive load, see figure below				
Bandwidth, lower limit	half power limit	100			Hz
Bandwidth, upper limit	half power limit			16,000	Hz
Overall gain	Inductive load, see figure below	TBD	20	TBD	dB
Output Noise	total rms voltage, 100-10kHz		71	TBD	μV
Total harmonic distortion	200 < f < 10kHz, Vin = 100 mVp-p 100Ω load, preamp at 13 dB gain		0.5	1	%
Total harmonic distortion	200 < f < 10kHz, Vin = 200 mVp-p 100Ω load, preamp at 13 dB gain		1.5	3	%
Total harmonic distortion	200 < f < 10kHz, Vin = 250 mVp-p 100Ω load, preamp at 13 dB gain		10		%
Total harmonic distortion	F = 1 kHz, Vin = 250 mVp-p, 100Ω load, preamp at max gain		TBD	TBD	%
Gain variation vs. Vcc	1.1 ≤ Vcc ≤ 1.4 volts		0.2	TBD	dB
Preamplifier					
Gain [20*log(V _{PAO} /V _{IN})]	PAO pad open		15		
Gain cut (relative to gain with PAO open)	PAI and PAO pads shorted	30	32		dB
Input resistance		35k	50k	65k	ohm
Output Stage					
Gain	Inductive load, see figure below	TBD	5	--	dB
Output drive transistors "ON" resistance	Total resistance through both FETs of the conducting part of the bridge		25		ohms
Free running oscillator frequency	no input, 1.1 ≤ Vcc ≤ 1.4 volts	100	120	150	kHz.
Duty cycle	No input, 100Ω resistive load	49	50	51	%

Items in grey are tested on a 100% basis at production.

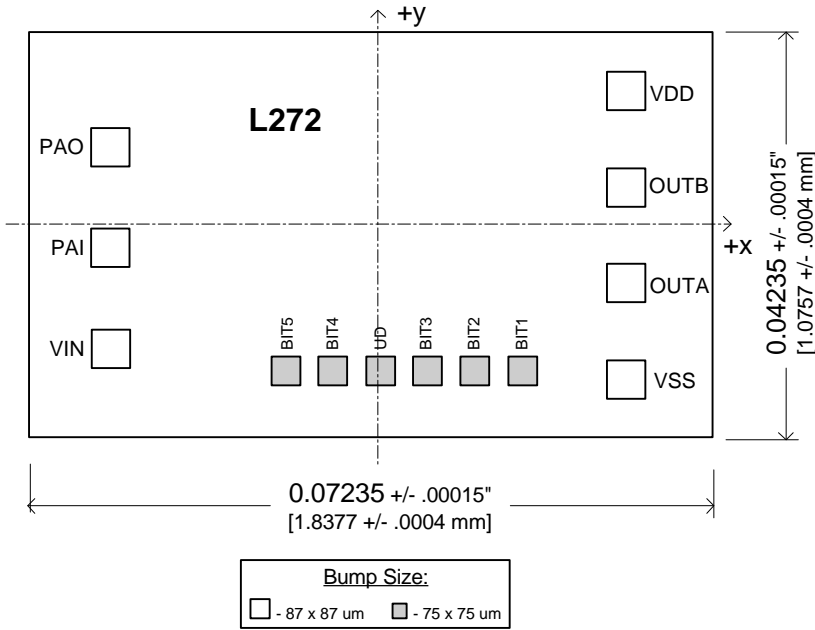
Simulated Receiver Load



Typical Characteristics



Mechanical View of L272 IC - Gold Bump Version, pn 80525-000



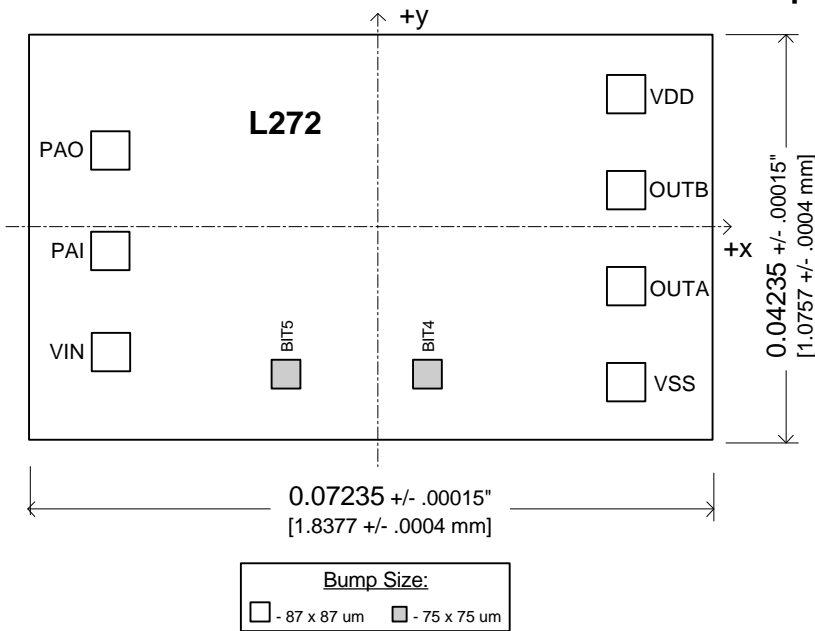
Pad positions

(center of pad relative to center of IC, in inches) * test pads

Name	X coord.	Y coord.
VSS	0.0266	-0.0151
OUTA	0.0266	-0.0051
OUTB	0.0266	+0.0049
VDD	0.0266	+0.0149
PAO	-0.0271	+0.0091
PAI	-0.0271	-0.0014
VIN	-0.0271	-0.0119
BIT5*	-0.0088	-0.0142
BIT4*	-0.0039	-0.0142
UD*	0.0010	-0.0142
BIT3*	0.0059	-0.0142
BIT2*	0.0108	-0.0142
BIT1*	0.0158	-0.0142

Die thickness: 0.013" +/- .001"
 [0.33 mm +/- .025mm]

Mechanical View of L272 IC - Gold Bump Version, pn 80525-002



Pad positions

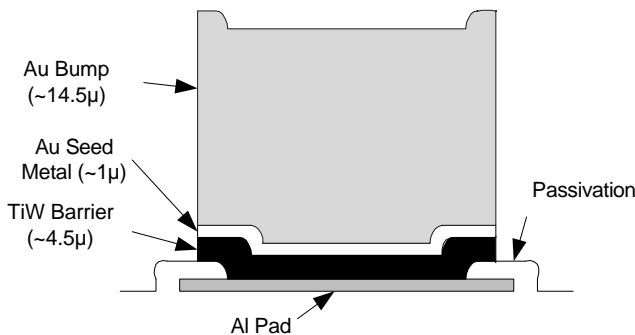
(center of pad relative to center of IC, in inches)

* test pads

Name	X coord.	Y coord.
VSS	0.0266	-0.0151
OUTA	0.0266	-0.0051
OUTB	0.0266	+0.0049
VDD	0.0266	+0.0149
PAO	-0.0271	+0.0091
PAI	-0.0271	-0.0014
VIN	-0.0271	-0.0119
BIT5*	-0.0088	-0.0142
BIT4*	0.0059	-0.0142

Die thickness: 0.013" +/- .001"
 [0.33 mm +/- .025mm]

Gold Bump Cross Section



Other Bump Specs:

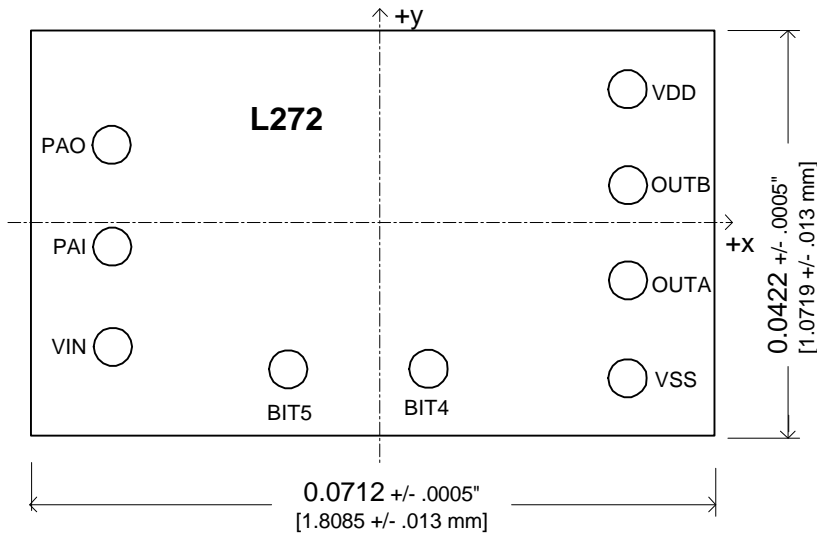
Bump Height = 20 ± 3µm
 Hardness = (35-65) HV10 after anneal using 10 g loading hardness test.

Shear Strength = 5.0 grams/mil² of bump area.

Layer Quality = 400°C for 30 minutes.

Bump Wall Slope = (80 ± 5) ° angle

Mechanical View of L272 IC - Solder Bump Version, pn 80525-001



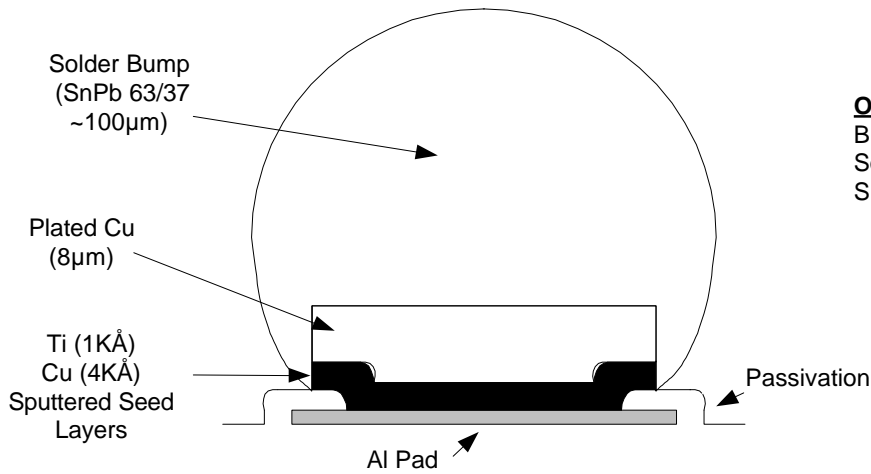
Pad positions

(center of pad relative to center of IC, in inches)
* test pads

Name	X coord.	Y coord.
VSS	0.0266	-0.0151
OUTA	0.0266	-0.0051
OUTB	0.0266	+0.0049
VDD	0.0266	+0.0149
PAO	-0.0271	+0.0091
PAI	-0.0271	-0.0014
VIN	-0.0271	-0.0119
BIT5*	-0.0088	-0.0142
BIT4*	0.0059	-0.0142

Die thickness: 0.019" +/- .001"
[0.48 mm +/- .025mm]

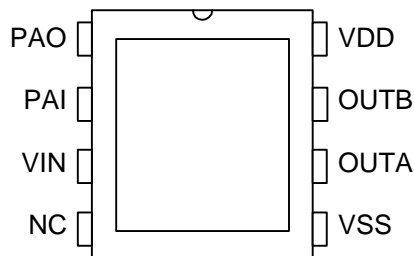
Typical Solder Bump Profile



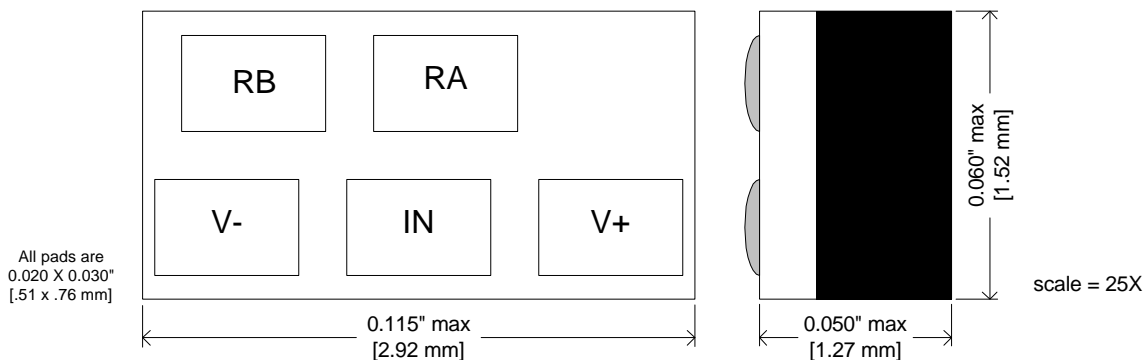
Other Bump Specs:

Bump Height = 100 µm nominal
Solder Type: Sn Pb 63/37
Shear Strength = 2.0 grams/mil² of bump area.

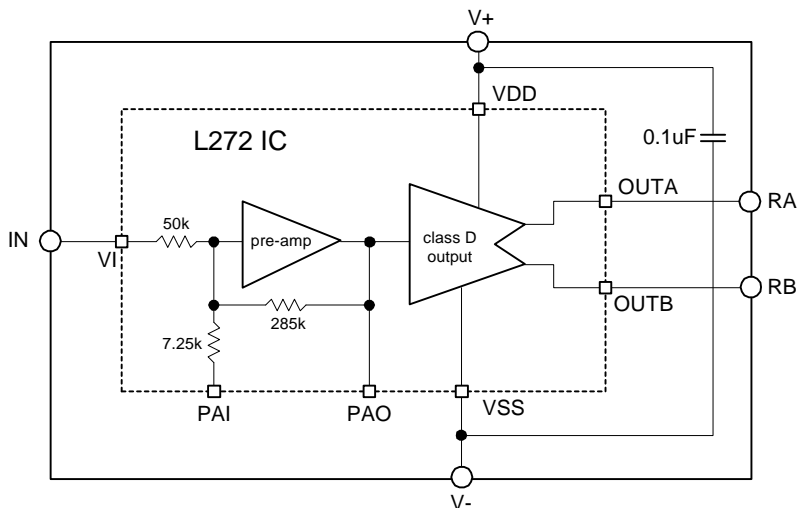
Dual In-line Package



Hybrid Package, part nr. 91098-000



Hybrid Schematic



Typical Application

